REMARKS

In response to the Final Office Action dated January 19, 2007, claims 1-5 are cancelled without prejudice. Claims 6-16 are now active in this application. No amendments have been made to claims 6-16. Thus, Applicant respectfully submits that no new issues are raised.

Applicant appreciates the Examiner's indication of allowable subject matter in claims 15 and 16, at pages 18 and 19 of the Office Action. Claims 15 and 16 are objected to, but would be allowable if rewritten in independent form including all of the limitations of the base claim.

Claims 1-5 were rejected under 35 U.S.C. § 102(e) as being anticipated by Tang et al. (U.S. Patent Publication 2004/0070440). Applicant respectfully submits that this rejection is moot because claims 1-5 have been cancelled.

Claims 1-5 and 13-14 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kaenel et al. (U.S. Patent 5,682,118). Applicant respectfully submits that this rejection is moot with respect to cancelled claims 1-5, and traverses this rejection with respect to claims 13 and 14.

Claims 6-9 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang in view of Forbes et al. (U.S. Patent 6,456,157). Applicant respectfully traverses this rejection.

Claims 10 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang in view of Forbes and further in view of Bowden (U.S. Patent 4,427,935). Applicant respectfully traverses this rejection.

Independent claim 6 recites, in pertinent part, "a current-voltage conversion circuit including a MOS transistor provided therein and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided

therein for converting a constant current value of the constant current generation circuit to a voltage value."

In order to establish *prima facie* obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. *In re Rokya*, 490 F. 2d 981, 180 USPQ 580 (CCPA 1974). At a minimum, the cited prior art does not disclose (expressly or inherently) the above recited limitation.

The Office Action, at page 9, admits that Tang fails to teach the above recited limitation. The Office Action asserts that Forbes discloses the above recited limitation referring to n-channel transistor 101 of FIG. 3. Forbes, at column 4, lines 8-13, merely states, "[a]s a consequence of the current source 100 forcing current into the drain, the backgate becomes forward biased and adjusts the backgate bias voltage V_{BG}. The backgate bias voltage is adjusted to a value which provides a threshold voltage value required to support the drain current I_D. The threshold voltage will be less than the reference potential V_{REF} and the transistor will turn on."

In contrast to Forbes, independent claim 6 recites, "a current-voltage conversion circuit including a MOS transistor provided therein and having **current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor** provided therein for converting a constant current value of the constant current generation circuit to a voltage value." Emphasis added. Note that Forbes, at FIG. 3, only has two inputs: V_{REF} and V_{DD}. Hence, Forbes has no way of knowing what the substrate potential is, and no way of changing current-voltage conversion characteristics according to the substrate potential of the MOS transistor. None of the other cited references obviate the deficiencies of Forbes.

Additionally, The Office Action asserts, at page 10, that it would have been "obvious" to replace the generic bias voltage generating circuits that output Vbs in FIGs. 1, 2, and 4 of Tang

et al. with the specific body bias generation circuits of FIGs. 3 and 4 of Forbes et al. for the purpose of having a simply constructed body bias generating circuit that outputs a body bias voltage and have increased flexibility in setting threshold voltages.

However, in contrast to Tang and Forbes, independent claim 6 recites a substrate potential control circuit, which includes a current-voltage conversion circuit and a differential amplifier circuit. As recited by claim 6, the differential amplifier circuit controls the substrate potential of the current voltage conversion circuit. Forbes does not disclose the use of a differential amplifier circuit in the circuitry citied in the Office Action as corresponding to the substrate potential control circuit. As such, if Tang is modified to include the circuitry of Forbes as suggested by the Office Action, the resulting circuit still fails to disclose a substrate potential control circuit having, in part, a differential amplifier circuit as recited by claim 6.

Further, the recited current-voltage conversion circuit includes a MOS transistor configured to have current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein for converting a constant current value of the constant current generation circuit to a voltage value. In other words, independent claim 6 does not merely flexibly set a threshold voltage. Instead, independent claim 6 recites a current-voltage conversion circuit with current-voltage conversion characteristics that change according to the substrate potential. Neither Tang, nor Forbes, independently or in combination, teach this recited limitation.

Thus, Applicant respectfully submit that independent claim 6 is distinguished over the cited references for at least the above reasons.

Independent claim 13 recites, in pertinent part, "the power supply voltage control circuit controls a voltage value of the operating power supply voltage supplied to the main circuit so

that an actual saturation current value of the MOS transistors in the main circuit is equal to the target saturation current value." At a minimum, the cited prior art does not disclose (expressly or inherently) the above recited limitation.

The Office Action, at page 7, asserts that the above recited limitation is disclosed by Kaenel at FIG. 7. However, Kaenel, at column 8, lines 14-49, merely states:

> FIG. 7 shows an example of a slaved system according to the invention employing a control circuit according to FIG. 4d and another one according to FIG. 8a. In this case, the ratio between the dynamic current and the static current consumed by a logic circuit is slaved. This makes it possible to optimize the threshold voltages of the MOS transistors constituting the logic circuit as a function of the level of activity of the latter.
>
> The slaving system 100 represented in FIG. 7 indirectly measures the activity of the logic circuit via the dynamic current consumed and takes a fraction thereof as static current datum for the well voltage control circuits.
>
> The ratio between these two quantities can be determined from the architecture and from the topology of the logic circuit.
>
> The slaving system 100 comprises two control circuits 101 and 102, a current measuring circuit 103 and a reduced-voltage source 104. The control circuit 101 comprises a comparator 105, a voltage-controlled oscillator 106, a multiplier 107, a resistor 108 and an n-type MOS transistor 109. These elements and their operation are identical to the corresponding elements described in connection with FIGS. 4a and 4b. The control circuit 101 also comprises a current source 111 and a voltage source 110 which will be described below.
>
> Likewise, the control circuit 102 comprises a comparator 112, a voltage-controlled oscillator 113, a multiplier 114, a resistor 115 and a p-type MOS transistor 116. These elements and their operation are identical to the corresponding elements and operation described in connection with FIG. 6.
>
> The control circuit 102 further comprises a current source 118 and a voltage source 117 which will also be described later.
>
> The slaving system 100 is intended to maintain the ratio between the dynamic power and the static power consumed by a logic circuit 119 at a defined value. The circuit may, for example, be the microprocessor of a portable computer or any circuit having a predetermined functionality.
>
> This logic circuit 119 comprises n-type MOS transistors, of which the MOS transistor 109 forms part and which are all created in a first well, and p-type MOS transistors, of which the MOS transistor 116 forms part and which are all created in a second well. The first and second wells are electrically isolated from one another.

Nowhere does the foregoing text of Kaenel teach or suggest "the power supply voltage control circuit controls a voltage value of the operating power supply voltage supplied to the main circuit so that an actual saturation current value of the MOS transistors in the main circuit is equal to the target saturation current value" as recited by independent claim 13. The other cited references do not obviate the deficiencies of Kaenel.

Thus, Applicant respectfully submits that independent claim 13 is distinguished over the cited references for at least the above reasons.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claims 6 and 13 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon (claims 9-12, and 14-16 respectively) are also patentable.

Thus, it is respectfully submitted that dependent claims 9-12, and 14-16 are also allowable.

Accordingly, it is urged that the application, as now amended, overcomes the rejection of record and is in condition for allowance. Entry of the amendment and favorable reconsideration of this application, as amended, are respectfully requested. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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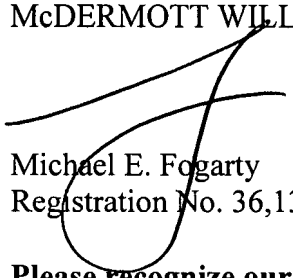

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